AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A method for maintaining an accurate frequency for a voltage controlled oscillator in a phase-locked loop, comprising the steps of:

receiving, at a phase detector, a phase input signal and a phase feedback signal from the voltage controlled oscillator;

measuring a pulse width property of ~~an~~ a first error signal output from the phase detector to obtain a pulse width property measurement;

storing the pulse width property measurement in a memory; and

~~generating~~selecting, depending upon a status of the phase input signal, one of a second error signal output from the phase detector and a new signal generated based on the stored pulse width property measurement for supply to the voltage controlled oscillator to maintain the frequency of the voltage controlled oscillator.

2. (Currently Amended) The method of claim 1, wherein the ~~generating step is performed~~ new signal is selected when the phase input signal is lost.

3. (Currently Amended) The method of claim 1, wherein the ~~generating step is performed~~ new signal is selected when the phase input signal becomes unsuitable for proper operation of the phase-locked loop.

4. (Original) The method of claim 1, wherein the measuring step is performed at periodic intervals.

5. (Original) The method of claim 1, wherein the measuring step is performed as an initial on-site calibration function.

6. (Original) The method of claim 1, wherein the phase input signal is derived from a reference clock signal.

7. (Currently Amended) The method of claim 1, wherein the pulse width property comprises a pulse width ~~measurement~~ of a high level of the first error signal and a pulse width ~~measurement~~ of a low level of the first error signal, and the measuring step further comprises the steps of:

detecting a first rising edge of the first error signal;

starting a counter to measure the high level pulse width of the first error signal;

detecting a falling edge of the first error signal;

stopping the counter to obtain the high level pulse width;

restarting the counter to measure the low level pulse width of the first error signal;

detecting a second rising edge of the first error signal; and

stopping the counter to obtain the low level pulse width.

8. (Currently Amended) The method of claim 1, wherein the pulse width property measurement comprises a high pulse width measurement of a high level of the first error signal and a pulse width measurement of a low level of the first error signal, and the new signal generation ~~generating step further~~ includes the steps of:

starting a ~~count-down~~ countdown counter from a count corresponding to the stored high level pulse width measurement;

generating a high level of the new signal until the counter stops;

restarting the counter to count down from a count corresponding to the stored low level pulse width measurement; and[[,]]

generating a low level of the new signal until the counter stops.

9. (Currently Amended) The method of claim 2, wherein ~~upon~~ in response to a reappearance of the phase input signal, the ~~generating step~~ supplying of the new signal is terminated.

10. (Currently Amended) The method of claim 3, wherein ~~upon~~ in response to acquiring a suitable phase input signal, the ~~generating step~~ supplying of the new signal is terminated.

11. (Currently Amended) A system comprising:

a phase detector that generates ~~an~~ a first error signal from a phase input signal and a phase feedback signal from a voltage controlled oscillator;

a measurement circuit ~~operative to measure~~ which measures a pulse width property of the first error signal;

a memory module ~~for storing~~ which stores the measured pulse width property; ~~and~~

a generation circuit ~~operative to retrieve~~ which retrieves the measured pulse width property from the memory module and ~~to generate~~ which generates a new signal based thereon; and

a selection circuit which selects, depending upon a status of the phase input signal, one of a second error signal and the new signal for supply to the voltage controlled oscillator to control the frequency of the voltage controlled oscillator.

~~wherein the new signal is used instead of the error signal to control the frequency of the voltage controlled oscillator.~~

12. (Currently Amended) A computer-readable medium containing a computer program for maintaining a frequency of a voltage controlled oscillator, said program including instructions for executing the steps of:

receiving, at a phase detector, a phase input signal and a phase feedback signal from the voltage controlled oscillator;

measuring a pulse width property of ~~an~~ a first error signal output from the phase detector to obtain a pulse width property measurement;

storing the pulse width property measurement in a memory; and

~~generating~~ selecting, depending upon a status of the phase input signal, one of a second error signal output from the phase detector and a new signal generated based on the stored pulse width property measurement for supply to the voltage controlled oscillator to phase-lock the voltage controlled oscillator.

13. (Currently Amended) The computer-readable medium of claim 12, ~~claim12,~~

wherein said step of measuring a pulse width property measures a duration of a high signal level and a duration of a low signal level of the first error signal, and said ~~step of generating a~~ generation of the new signal generates a high signal level for a time duration corresponding to the measured high signal level and generates a low signal level

for a time duration corresponding to the measured low signal level.

14. (Currently Amended) A method for calibrating a phase-locked loop circuit, comprising:

receiving ~~an input~~ a phase input signal and a feedback signal into a phase detector such that the loop is phase-locked;

measuring a pulse width property of ~~an~~ a first error signal output from the phase detector;

storing the measured pulse width property of the first error signal;

using the stored pulse width property to generate a calibration reference signal, which can be supplied to a voltage controlled oscillator; and

selectively supplying, to the voltage controlled oscillator, one of a second error signal output from the phase detector and the calibration reference signal, depending upon a status of the phase input signal. ~~the phase detector.~~

15. (Currently Amended) A method of implementing clock holdover in a phase-locked loop circuit, comprising:

receiving ~~an input~~ a phase input signal and a feedback signal into a phase detector such that the loop is phase-locked;

periodically measuring a pulse width property of an error signal output from the phase detector;

determining whether the measured pulse width property satisfies a predetermined condition over a predetermined period of time, and storing the measured pulse width property ~~if~~ depending upon whether it satisfies the predetermined condition; and

using the stored pulse width property to generate a ~~reference~~ new signal to be supplied to ~~the phase detector a~~ voltage controlled oscillator when the ~~input~~ phase input signal is lost or becomes unsuitable for proper operation of the phase-locked loop.

16. (Currently Amended) A method of qualifying a potential clock reference for a phase-locked loop circuit, said phase-locked loop circuit comprising a phase detector ~~having~~ which receives a phase input signal and a phase feedback signal, ~~as inputs,~~ a system clock, and a VCO, said method comprising:

a. determining a relative frequency measurement of the potential clock reference relative to the system clock;

b. measuring a pulse width property of an error signal output from the phase detector;

c. determining a frequency output of the VCO from the measured pulse width property; and

d. determining whether the potential clock reference would lock the phase-locked loop from the determined relative frequency measurement and the determined VCO frequency output.